Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. 1A**
2. **1B**
3. **N. 1R**
4. **N. 1Q**
5. **2Q**
6. **2CX**
7. **2RXCX**
8. **GND**
9. **N. 2A**
10. **2B**
11. **N. 2R**
12. **N. 2Q**
13. **1Q**
14. **1CX**
15. **1RXCX**
16. **VCC**

**.046”**

**2 1 16 15**

**7 8 9**

**3**

**4**

**5**

**6**

**14**

**13**

**12**

**11**

**10**

**MASK**

**REF**

**HCT**

**123T**

**.072”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VCC**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .046” X .072” DATE: 8/26/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54HCT123**

**DG 10.1.2**

#### Rev B, 7/1